



US 20110140112A1

(19) **United States**(12) **Patent Application Publication****Kim et al.**(10) **Pub. No.: US 2011/0140112 A1**(43) **Pub. Date: Jun. 16, 2011**(54) **ORGANIC LIGHT EMITTING DISPLAY AND
METHOD OF MANUFACTURING THE SAME****Publication Classification**(51) **Int. Cl.****H01L 51/52** (2006.01)**H01L 51/56** (2006.01)(52) **U.S. Cl. 257/59; 438/34; 257/E51.018**

(57)

ABSTRACT

An organic light emitting display and a method of manufacturing the same are disclosed. In one embodiment, the display includes a gate electrode formed over a substrate and an active layer electrically insulated from the gate electrode, wherein the gate electrode is closer to the substrate than the active layer. The display further includes i) a first gate insulating layer and a second gate insulating layer formed between the gate electrode and active layer so as to electrically insulate the active layer from the gate electrode and ii) source and drain electrodes each contacting the active layer.

(75) Inventors: **Min-Kyu Kim**, Yongin-city (KR);
Jae-Wook Kang, Yongin-city (KR)(73) Assignee: **Samsung Mobile Display Co.,
Ltd.**, Yongin-city (KR)(21) Appl. No.: **12/881,686**(22) Filed: **Sep. 14, 2010**(30) **Foreign Application Priority Data**

Dec. 16, 2009 (KR) 10-2009-0125685

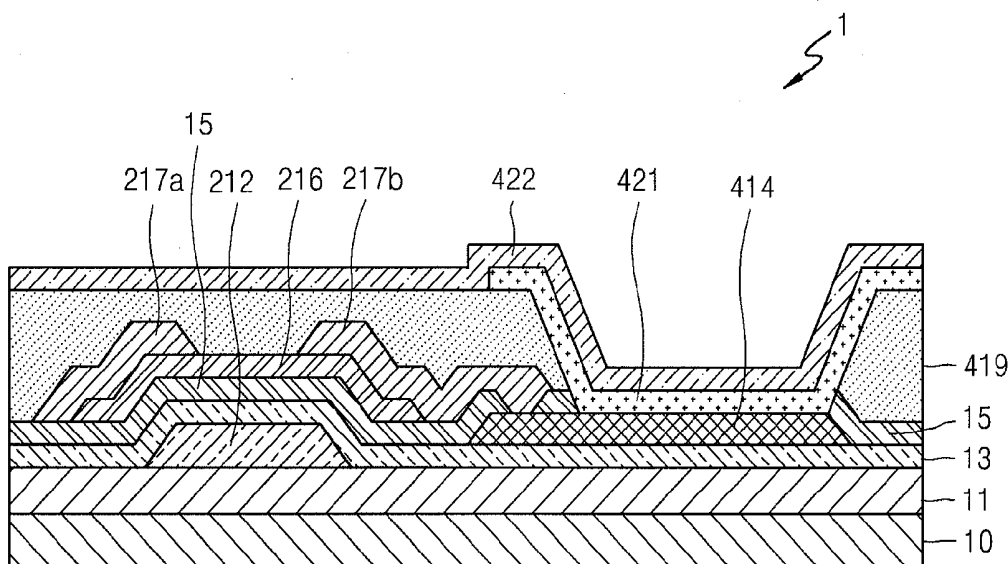


FIG. 1

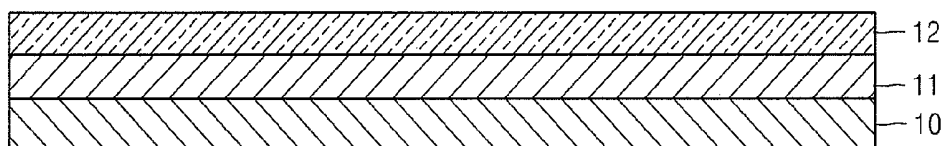


FIG. 2

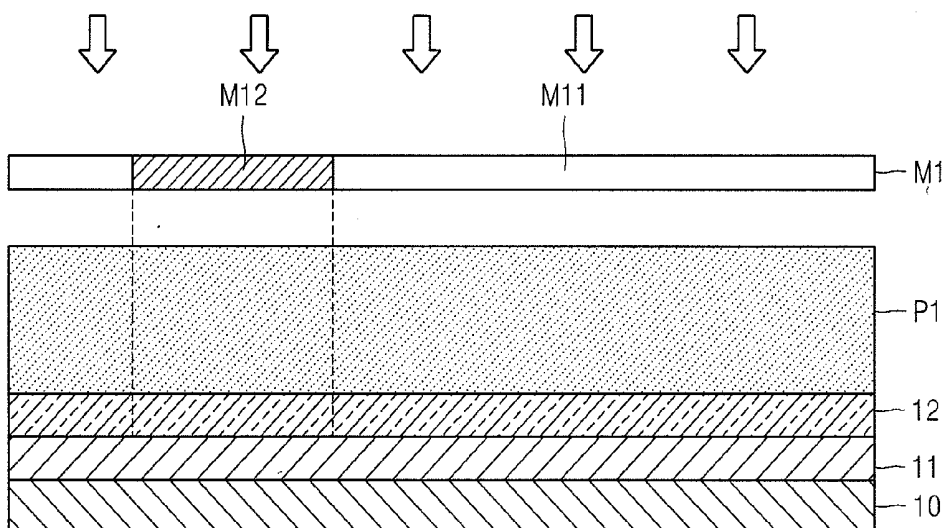


FIG. 3

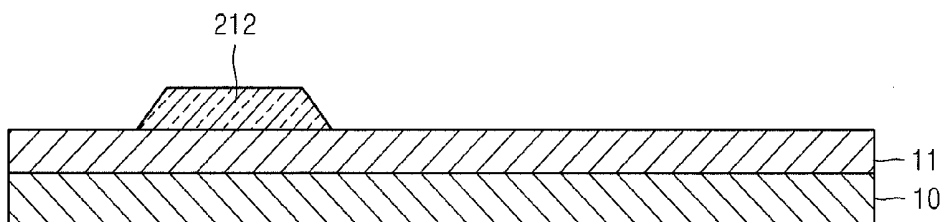


FIG. 4

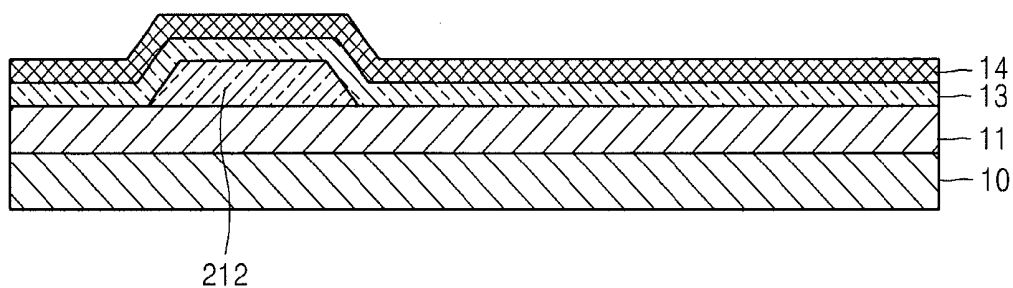


FIG. 5

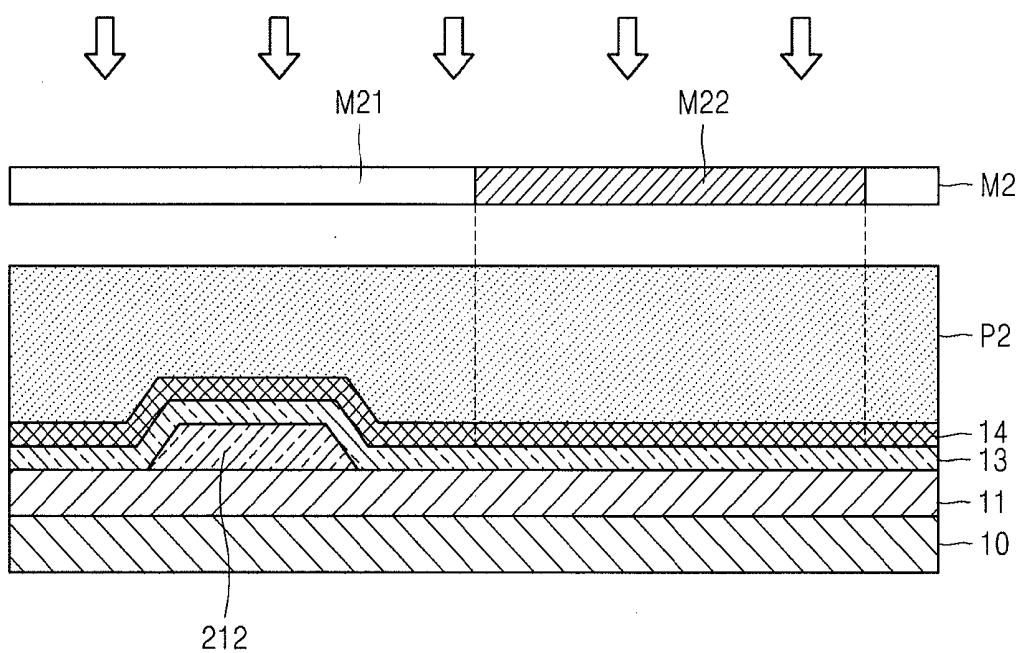


FIG. 6

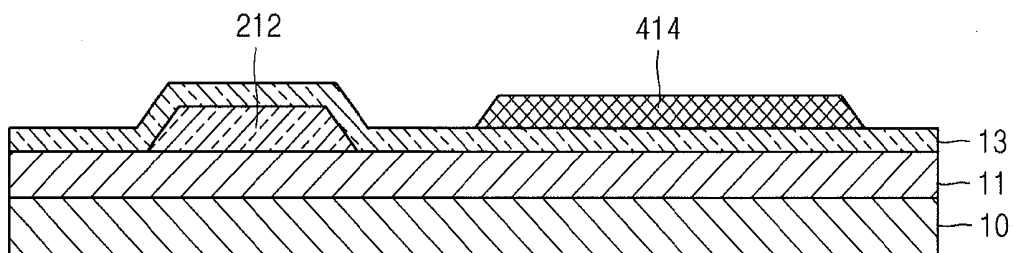


FIG. 7

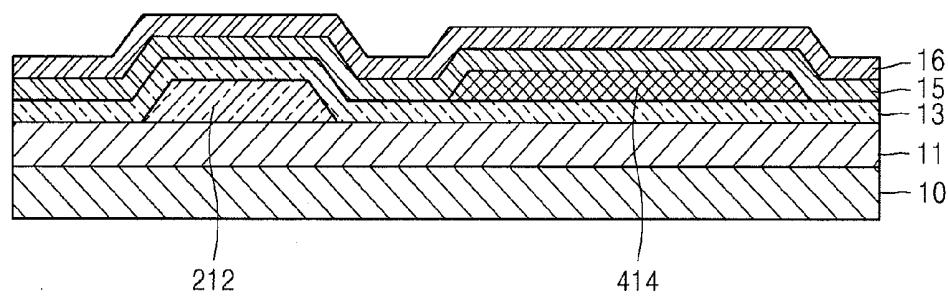


FIG. 8

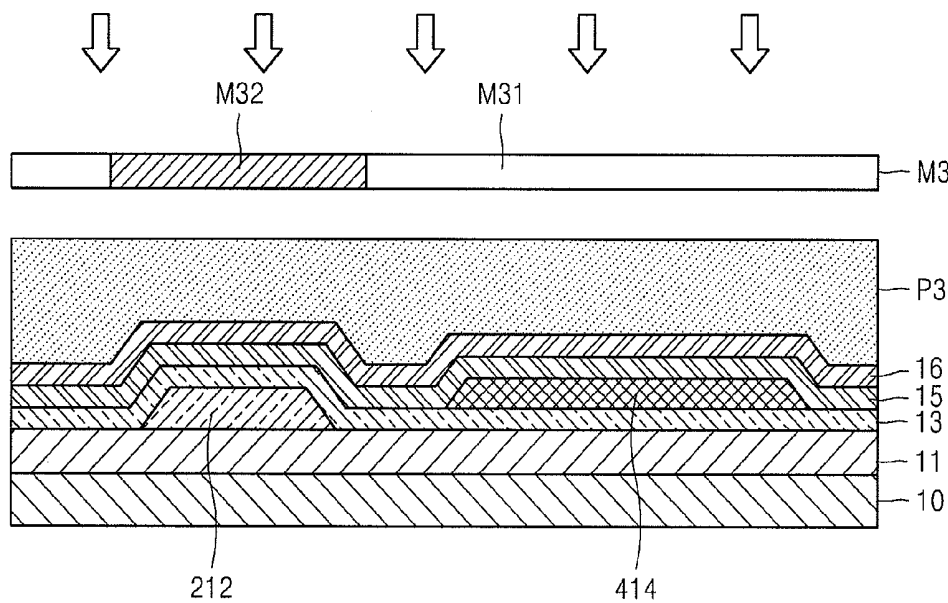


FIG. 9

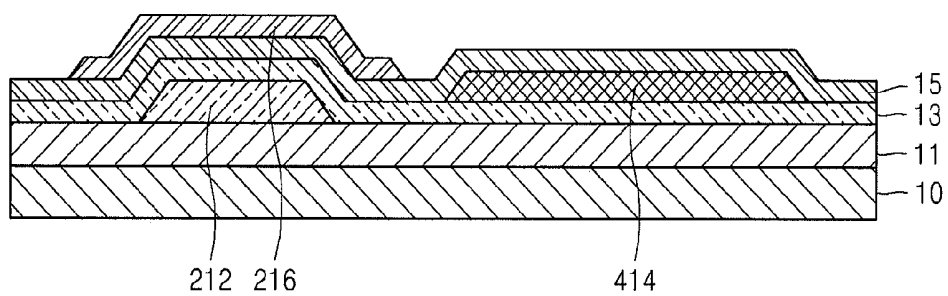


FIG. 10

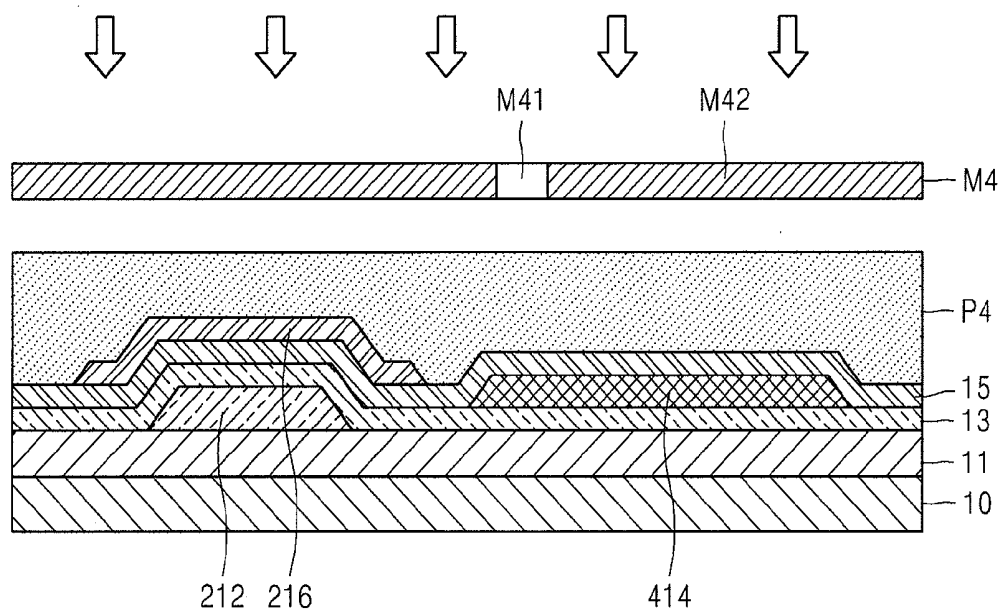


FIG. 11

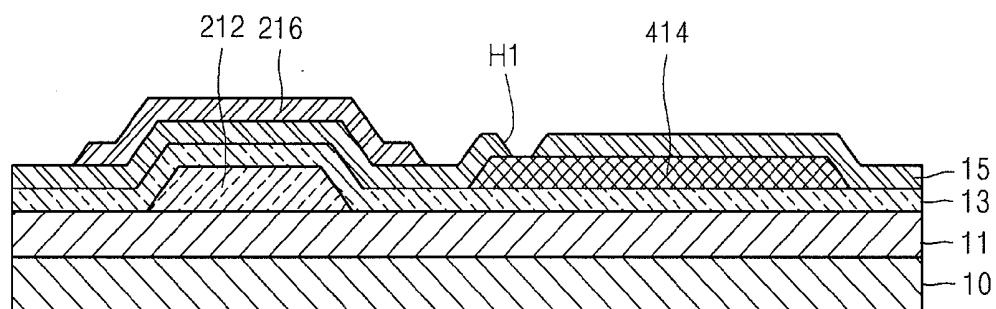


FIG. 12

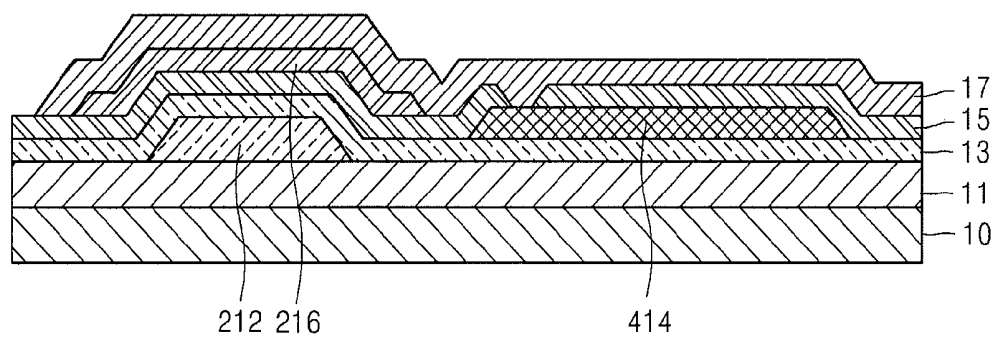


FIG. 13

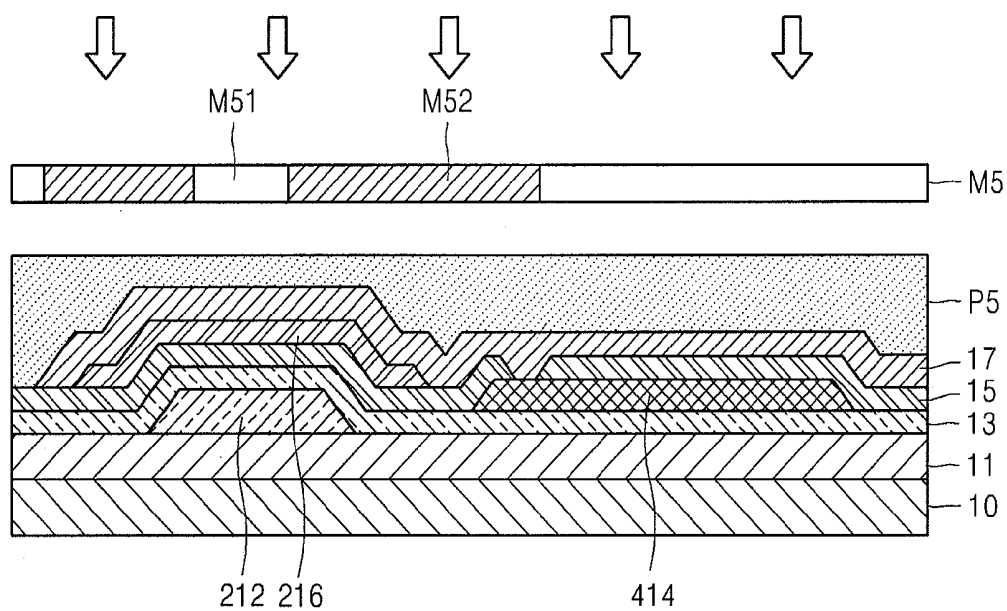


FIG. 14

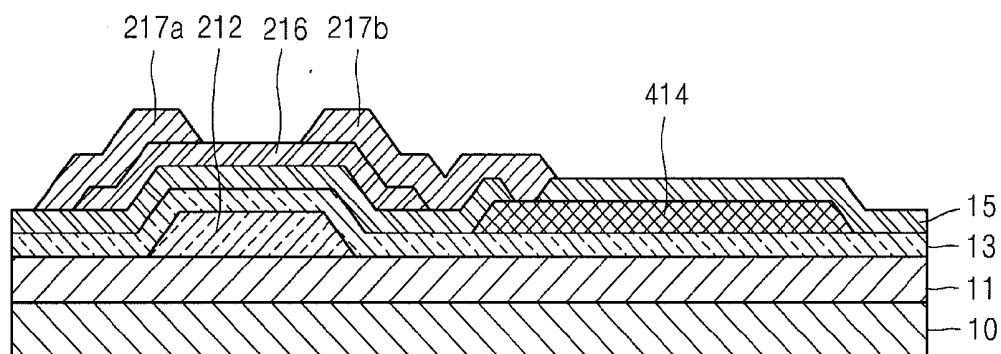


FIG. 15

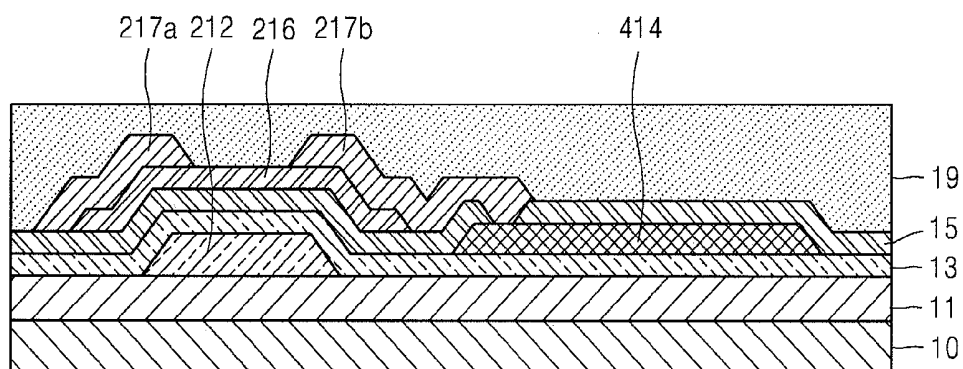


FIG. 16

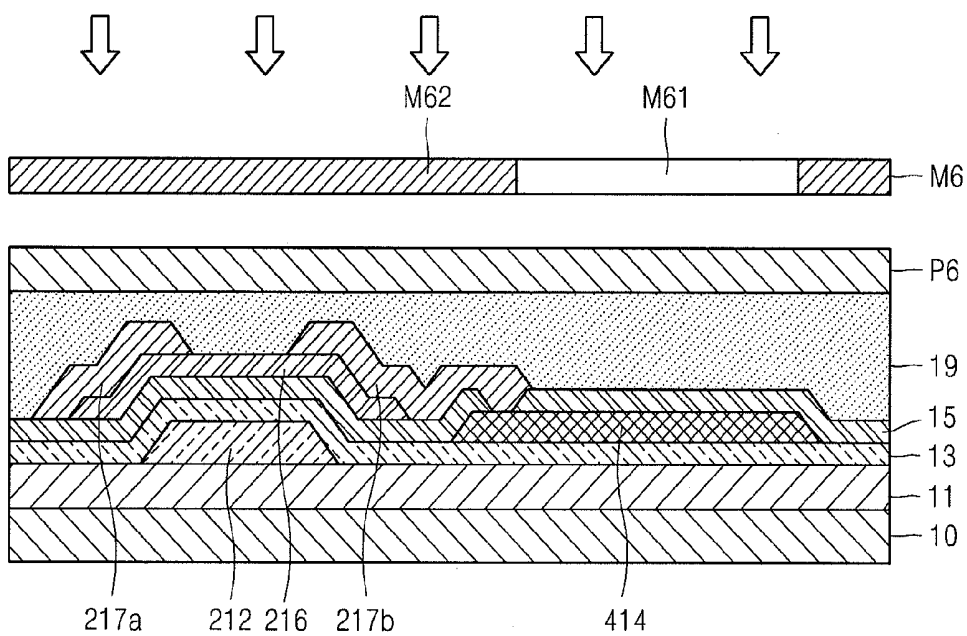


FIG. 17

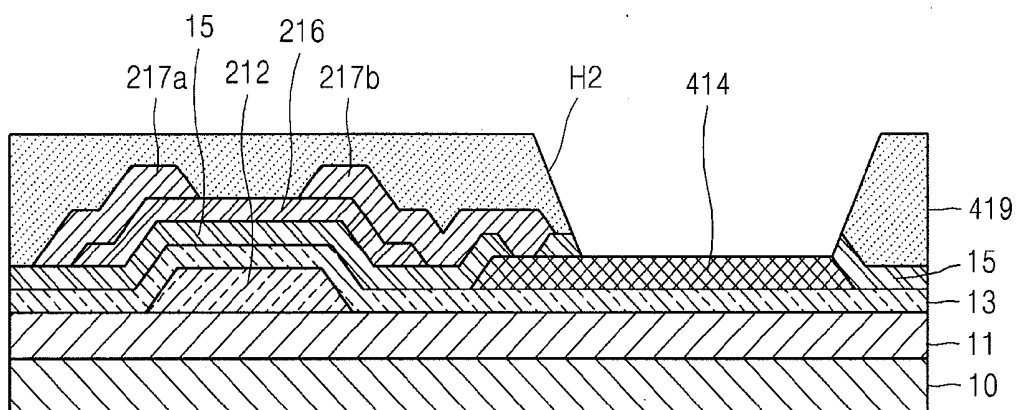
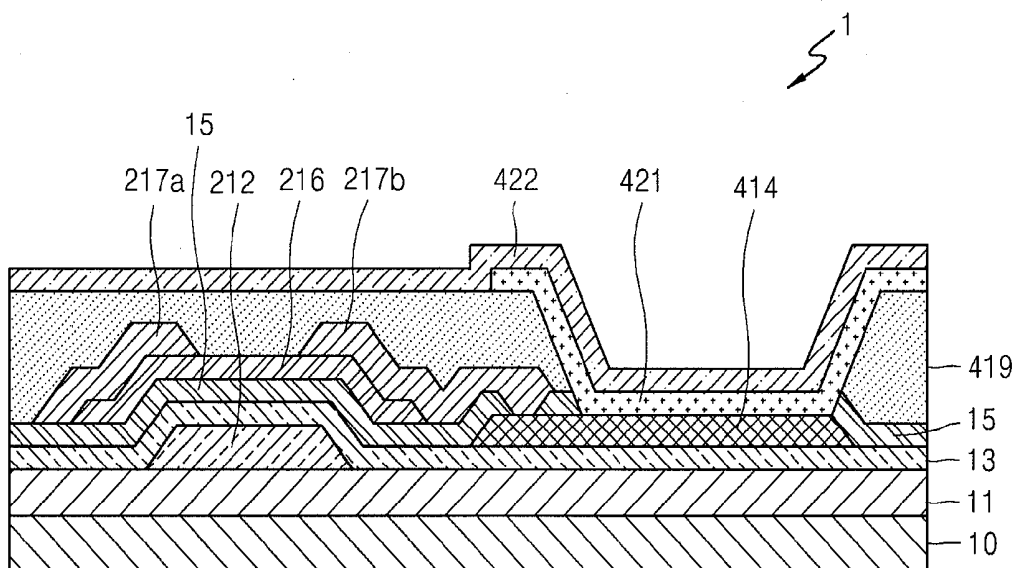


FIG. 18



**ORGANIC LIGHT EMITTING DISPLAY AND
METHOD OF MANUFACTURING THE SAME****CROSS-REFERENCE TO RELATED PATENT
APPLICATION**

[0001] This application claims the benefit of Korean Patent Application No. 10-2009-0125685, filed on Dec. 16, 2009, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] 1. Field

[0003] The described technology generally relates to an organic light emitting display and a method of manufacturing the same, and more particularly, to an organic light emitting display manufactured in a simple manufacturing process and a method of manufacturing the same.

[0004] 2. Description of the Related Technology

[0005] In flat panel displays, such as organic light emitting displays, liquid crystal displays, a substrate includes patterns of electrical components such as a thin film transistor, a capacitor, wiring connecting the components.

SUMMARY

[0006] One aspect is an organic light emitting display manufactured with a reduced number of patterning processes using a mask, and a method of manufacturing the same.

[0007] Another aspect is an organic light emitting display including: a gate electrode formed on a substrate; an active layer insulated from the gate electrode; a first gate insulating layer and a second gate insulating layer to insulate the gate electrode and the active layer; and source and drain electrodes respectively contacting the active layer.

[0008] The active layer may include oxygen and at least one selected from the group consisting of Ga, In, Zn, Hf, and Sn.

[0009] The first gate insulating layer and the second gate insulating layer may be formed adjacent to each other.

[0010] The organic light emitting display may further include: a plurality of pixel electrodes formed on the first gate insulating layer; pixel-defining layers disposed between the plurality of pixel electrodes; a plurality of organic layers disposed on the plurality of pixel electrodes and the pixel defining layers; and a counter electrode formed on the plurality of organic layers.

[0011] Another aspect is a method of manufacturing an organic light emitting display, the method comprising: a first mask process for forming a first conductive layer on a substrate and patterning the first conductive layer as a gate electrode of a thin film transistor; a second mask process for forming a first insulating layer on the resulting structure obtained according to the first mask process, forming a second conductive layer on the first insulating layer, and patterning the first insulating layer and the second conductive layer as a pixel electrode; a third mask process for forming a second insulating layer on the resulting structure obtained according to the second mask process, forming a semiconductor layer on the second insulating layer, and patterning the second insulating layer and the semiconductor layer as an active layer of the thin film transistor; a fourth mask process for removing a portion of the second insulating layer to expose a portion of the pixel electrode; a fifth mask process for forming a third conductive layer on the resulting structure obtained according to the fourth mask process and patterning the third conductive

layer as source and drain electrodes of the thin film transistor; and a sixth mask process for forming a third insulating layer on the resulting structure obtained according to the fifth mask process and removing the third insulating layer to expose the pixel electrode.

[0012] The active layer may include oxygen and at least one element selected from the group consisting of Ga, In, Zn, Hf, and Sn.

[0013] The first insulating layer may be formed as a first gate insulating layer, and the second insulating layer may be formed as a second gate insulating layer, wherein the first gate insulating layer and the second gate insulating layer are formed adjacent to each other.

[0014] The method may further include sequentially forming an intermediate layer comprising an emissive layer and a counter electrode on the resulting structure obtained according to the sixth mask process. The method may further include forming a buffer layer on the substrate.

[0015] Another aspect is an organic light emitting display comprising: a gate electrode formed over a substrate; an active layer electrically insulated from the gate electrode, wherein the gate electrode is closer to the substrate than the active layer; a first gate insulating layer and a second gate insulating layer formed between the gate electrode and active layer so as to electrically insulate the active layer from the gate electrode; and source and drain electrodes each contacting the active layer.

[0016] In the above display, the active layer is formed at least partially of oxygen and at least one selected from the group consisting of Ga, In, Zn, Hf, and Sn. In the above display, the first gate insulating layer and the second gate insulating layer are formed adjacent to each other. In the above display, the first gate insulating layer covers the gate electrode.

[0017] The above display further comprises: a plurality of pixel electrodes formed on the first gate insulating layer; a plurality of pixel-defining layers formed between the pixel electrodes; a plurality of organic layers formed on the pixel electrodes and the pixel defining layers; and a counter electrode formed on the organic layers.

[0018] In the above display, the second gate insulating layer contacts i) at least one of the pixel electrodes and ii) at least one of the pixel defining layers. In the above display, at least one of the organic layers contacts the second gate insulating layer. In the above display, the active layer contacts at least one of the pixel-defining layers. In the above display, the source and drain electrodes contact part of the second gate insulating layer.

[0019] Another aspect is a method of manufacturing an organic light emitting display, the method comprising: performing a first mask process so as to form a first conductive layer on a substrate and pattern the first conductive layer to form a gate electrode of a thin film transistor; performing a second mask process so as to form a first insulating layer on the resulting structure obtained according to the first mask process, form a second conductive layer on the first insulating layer, and pattern the second conductive layer to form a pixel electrode; performing a third mask process so as to form a second insulating layer on the resulting structure obtained according to the second mask process, form a semiconductor layer on the second insulating layer, and pattern the semiconductor layer to form an active layer of the thin film transistor; performing a fourth mask process so as to remove a portion of the second insulating layer to expose a portion of the pixel

electrode; performing a fifth mask process so as to form a third conductive layer on the resulting structure obtained according to the fourth mask process and pattern the third conductive layer to form source and drain electrodes of the thin film transistor; and performing a sixth mask process so as to form a third insulating layer on the resulting structure obtained according to the fifth mask process and remove the third insulating layer to expose the pixel electrode.

[0020] In the above method, the active layer is formed at least partially of oxygen and at least one element selected from the group consisting of Ga, In, Zn, Hf, and Sn. In the above method, the first insulating layer is formed as a first gate insulating layer, wherein the second insulating layer is formed as a second gate insulating layer, and wherein the first gate insulating layer and the second gate insulating layer contact each other. The above method further comprises sequentially forming i) an intermediate layer comprising an emissive layer and ii) a counter electrode on the resulting structure obtained according to the sixth mask process. The above method further comprises forming a buffer layer between the substrate and the gate electrode, wherein the buffer layer contacts the first gate insulating layer.

[0021] Another aspect is an organic light emitting display comprising: a gate electrode formed over a substrate; a first gate insulating layer substantially covering the gate electrode; a second gate insulating layer formed on the first gate insulating layer; an active layer formed over and contacting the second gate insulating layer; and source and drain electrodes formed over and contacting the active layer.

[0022] The above display further comprises: a pixel electrode formed on the first gate insulating layer, wherein at least part of the pixel electrode is interposed between the first and second gate insulating layers; an organic light emission layer formed on the pixel electrode; and a counter electrode formed on the organic light emission layer.

[0023] The above display further comprises a pixel-defining layer formed between the second gate insulating layer and organic light emission layer, wherein the pixel-defining layer covers i) the source and drain electrodes, ii) part of the active layer and iii) part of the second gate insulating layer. In the above display, the first and second gate insulating layers have substantially the same thickness.

[0024] In the above display, the active layer covers at least part of the second gate insulating layer, and wherein the active layer is farther from the substrate than the first and second gate insulating layers. In the above display, the first gate insulating layer does not contact the pixel-defining layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] FIGS. 1 through 17 are schematic cross-sectional views sequentially illustrating a method of manufacturing an organic light emitting display, according to an embodiment.

[0026] FIG. 18 is a schematic cross-sectional view of an organic light emitting display manufactured using the method illustrated in FIGS. 1 through 17, according to an embodiment.

DETAILED DESCRIPTION

[0027] In general, to form micro-patterns of electrical components such as a thin film transistor on the substrate used in flat panel displays, micro-patterns formed in masks are transferred to a substrate. For this process, a photolithography process is generally used. The photolithography process is

performed as follows: a substrate to be patterned is uniformly coated with a photoresist, the photoresist is exposed to light using a mask with patterns and by using exposure equipment such as a stepper, and the photoresist is developed (when a positive photoresist is used). In addition, after the photoresist is developed, patterns are etched using the remaining photoresist as a mask, and the unnecessary photoresist is removed.

[0028] In the process of transferring patterns using a mask, a mask with desired patterns is needed, and thus as the number of processes using a mask increases, the manufacturing costs for the masks increases. In addition, due to the complicated operations described above, the manufacturing processes are complicated, the manufacturing time increases, and the manufacturing costs are high.

[0029] Embodiments will now be described in more detail with reference to the accompanying drawings.

[0030] Referring to FIGS. 1 through 18, the organic light emitting display 1 according to an embodiment includes a substrate 10, a buffer layer 11 (See FIG. 1), a thin film transistor 2, and an organic light emitting diode 4 (See FIG. 18).

[0031] Referring to FIG. 1, the buffer layer 11 and a first conductive layer 12 are sequentially formed on the substrate 10.

[0032] The substrate 10 may be formed at least partially of a transparent glass material including SiO₂ as a main component. Also, the substrate 10 may be formed at least partially of an opaque material, or other materials, such as plastic. In a bottom emission type organic light emitting display in which an image is displayed through the substrate 10, the substrate 10 may be formed at least partially of a transparent material.

[0033] The buffer layer 11 may be formed on the substrate 10 to provide the substrate 10 with a smooth surface and prevent impurity elements from penetrating into the substrate 10. The buffer layer 11 may be formed by depositing, for example, SiO₂ and/or SiN_x on the substrate 10 by, for example, plasma enhanced chemical vapor deposition (PECVD), atmospheric pressure CVD (APCVD), or low pressure CVD (LPCVD).

[0034] The first conductive layer 12 is formed on the buffer layer 11. The first conductive layer 12 may be formed of at least one transparent material selected from the group consisting of ITO, IZO, ZnO, and In₂O₃. The first conductive layer 12 may also be formed of at least one material selected from the group consisting of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, MoW, and Al/Cu. The first conductive layer 12 is used to form a gate electrode 212 of the thin film transistor 2 (See, for example, FIG. 17), which will be described later.

[0035] Referring to FIG. 2, a first photoresist layer P1 is formed on the resulting structure of FIG. 1 by coating the structure of FIG. 1 with a photoresist and pre-baking or soft-baking the photoresist to remove the solvent. Next, to pattern the first photoresist layer P1, a first mask M1 with a predetermined pattern is substantially aligned with the substrate 10. The first mask M1 includes a light transmitting portion M11 and a light blocking portion M12. The light transmitting portion M11 transmits light in a predetermined wavelength range, and the light blocking portion M12 blocks the irradiated light. Subsequently, the first photoresist layer P1 is exposed to light irradiated thereto in a predetermined wavelength range. In the present embodiment, a positive photoresist (positive PR) is used to remove regions exposed to light; however, a negative PR may also be used.

[0036] When the first photoresist layer P1 is exposed to light, a portion of the first photoresist layer P1 formed substantially directly below the light transmitting portion M11 of the first mask M1 is removed, and a portion of the first photoresist layer P1 formed substantially directly below the light blocking portion M12 of the first mask M1 remains. Using the patterns of the first photoresist layer P1 as a mask, the first conductive layer 12 is etched using an etching device. In this manner, a portion of the first conductive layer 12 is etched, and a non-etched portion of the first conductive layer 12 is formed as the gate electrode 212 of the thin film transistor 2, as illustrated in FIG. 3.

[0037] Referring to FIG. 4, a first insulating layer 13 and a second conductive layer 14 are sequentially formed on the resulting structure of FIG. 3 obtained according to the first mask process.

[0038] The first insulating layer 13 may be formed by depositing an inorganic material such as SiN_x or SiO_x on the resulting structure of FIG. 3 by, for example, PECVD, APCVD, or LPCVD. The first insulating layer 13 is disposed between the gate electrode 212 of the thin film transistor 2 and an active layer 216 (See, for example, FIG. 9), which will be described later, to function as a first gate insulating layer of the thin film transistor 2.

[0039] The second conductive layer 14 may be formed of at least one transparent material selected from the group consisting of ITO, IZO, ZnO, and In_2O_3 . The second conductive layer 14 is used to form a pixel electrode 414 (See FIG. 6) of the organic light emitting display 1, which will be described later.

[0040] Next, referring to FIG. 5, a second photoresist layer P2 is formed on the second conductive layer 14, and a second mask M2 is substantially aligned with the substrate 10.

[0041] Referring to FIG. 5, the second photoresist layer P2 is formed on the resulting structure of FIG. 4 by coating the resulting structure of FIG. 4 with a photoresist and pre-baking or soft-baking the photoresist to remove the solvent. Next, to pattern the second photoresist layer P2, the second mask M2 with a predetermined pattern is substantially aligned with the substrate 10. The second photoresist layer P2 is then exposed to light by irradiating light in a predetermined wavelength range thereto.

[0042] When the second photoresist layer P2 is exposed to light, a portion of the second photoresist layer P2 formed substantially directly below a light transmitting portion M21 of the second mask M2 is removed, and a portion of the second photoresist layer P2 formed substantially directly below a light blocking portion M22 of the second mask M2 remains. Using the patterns of the photoresist layer P2 as a mask, the second conductive layer 14 is etched using an etching device. In this manner, a portion of the second conductive layer 14 is etched, and a non-etched portion of the second conductive layer 14 is formed as the pixel electrode 414 of the organic light emitting display 1, as illustrated in FIG. 6.

[0043] Referring to FIG. 7, a second insulating layer 15 and a semiconductor layer 16 are sequentially formed on the resulting structure of FIG. 6 obtained according to the second mask process.

[0044] The second insulating layer 15 may be formed by depositing an inorganic material such as SiN_x or SiO_x on the resulting structure of FIG. 6 by, for example, PECVD, APCVD, or LPCVD. The second insulating layer 15 is disposed between the gate electrode 212 of the thin film transistor

2 and the active layer 216 (see, for example, FIG. 9), which will be described later, to function as a second gate insulating layer of the thin film transistor 2. In one embodiment, the first and second gate insulating layers 13 and 15 may have substantially the same thickness. In another embodiment, the first and second gate insulating layers 13 and 15 have different thicknesses.

[0045] The semiconductor layer 16 may be formed at least partially of an oxide. For example, the semiconductor layer 16 may be formed at least partially of oxygen and at least one element selected from the group consisting of Ga, In, Zn, Hf, and Sn. As another example, the semiconductor layer 16 may be formed at least partially of ZnO, ZnGaO, ZnInO, GaInO, GaSnO, ZnSnO, InSnO, ZnGaInO, or HfInZnO. The semiconductor layer 16 is used to form the active layer 216 of the thin film transistor 2, which will be described later.

[0046] Referring to FIG. 8, a third photoresist layer P3 is formed on the semiconductor layer 16, and a third mask M3 is substantially aligned with the substrate 10.

[0047] The third photoresist layer P3 may be formed on the resulting structure of FIG. 7 by coating the structure of FIG. 7 with a photoresist and pre-baking or soft-baking the photoresist to remove the solvent. Next, to pattern the third photoresist layer P3, the third mask M3 with a predetermined pattern is substantially aligned with the substrate 10. The third photoresist layer P3 is then exposed to light by irradiating light in a predetermined wavelength range thereto.

[0048] When the third photoresist layer P3 is exposed to light, a portion of the third photoresist layer P3 formed substantially directly below a light transmitting portion M31 of the third mask M3 is removed, and a portion of the third photoresist layer P3 formed substantially directly below a light blocking portion M32 of the third mask M3 remains. Using the patterns of the third photoresist layer P3 as a mask, the semiconductor layer 16 is etched using an etching device. In this manner, a portion of the semiconductor layer 16 is etched, and a non-etched portion of the semiconductor layer 16 is formed as the active layer 216 of the thin film transistor 2, as illustrated in FIG. 9.

[0049] Referring to FIG. 10, a fourth photoresist layer P4 is formed on the resulting structure of FIG. 9 obtained according to the third mask process, and then a fourth mask M4 is substantially aligned with the substrate 10.

[0050] The fourth mask M4 includes a light transmitting portion M41 corresponding to a portion of the pixel electrode 414 and a light blocking portion M42. Using the fourth mask M4 substantially aligned with the substrate 10, the fourth photoresist layer P4 is exposed to light.

[0051] Referring to FIG. 11, the resulting structure of FIG. 11 is obtained such that after portions of the fourth photoresist layer P4 exposed to light are removed, the resulting structure is etched using the remaining patterns of the fourth photoresist layer P4 as a mask, thereby resulting in forming a hole H1 in the second insulating layer 15, which exposes a portion of the pixel electrode 414.

[0052] Referring to FIG. 12, a third conductive layer 17 is formed on the resulting structure of FIG. 11 obtained according to the fourth mask process. The third conductive layer 17 may be formed by depositing an amorphous silicon, including N-type or P-type impurities, on the resulting structure of FIG. 11 and heat treating the amorphous silicon. The third conductive layer 17 is patterned as a source region 217a and a drain region 217b of the thin film transistor 2 (see, for example, FIG. 14).

[0053] Next, referring to FIG. 13, a fifth photoresist layer P5 is formed on the third conductive layer 17, and a fifth mask M5 is substantially aligned with the substrate 10.

[0054] The fifth photoresist layer P5 may be formed by coating the resulting structure of FIG. 12 with a photoresist and pre-baking or soft-baking the photoresist to remove the solvent. Then, to pattern the fifth photoresist layer P5, the fifth mask M5 with a predetermined pattern is substantially aligned with the substrate 10, and the fifth photoresist layer P5 is exposed to light by irradiating light in a predetermined wavelength range thereto.

[0055] As a result of the light exposure process, a portion of the fifth photoresist layer P5 formed substantially directly below a light transmitting portion M51 of the fifth mask M5 is removed, and a portion of the fifth photoresist layer P5 formed substantially directly below a light blocking portion M52 of the fifth mask M5 remains. Using the patterns of the fifth photoresist layer P5 as a mask, the third conductive layer 17 is etched using an etching device. In this manner, a portion of the third conductive layer 17 is etched, and a non-etched portion of the third conductive layer 17 is formed as the source region 217a and the drain region 217b of the thin film transistor 2.

[0056] Referring to FIG. 15, a third insulating layer 19 is formed on the resulting structure of FIG. 14 obtained according to the fifth mask process.

[0057] The third insulating layer 19 may be formed at least partially of at least one organic insulating material selected from the group consisting of polyimide, polyamide, an acryl resin, benzocyclobutene and a phenol resin by using a spin coating method. The third insulating layer 19 may also be formed at least partially of an inorganic insulating material used to form the first insulating layer 13 and the second insulating layer 15. The third insulating layer 19 acts as a pixel defining layer of the organic light emitting display, which will be described later, after an etching process using a sixth mask M6.

[0058] Next, referring to FIG. 16, a sixth photoresist layer P6 is formed on the third insulating layer 19, and a sixth mask M6 is substantially aligned with the substrate 10.

[0059] The sixth mask M6 includes a light transmitting portion M61 corresponding to the pixel electrode 414 and a light blocking portion M62. When light is irradiated to the sixth mask M6, the organic insulating material of a portion of the third insulating layer 19 through which the light is transmitted may be directly removed by dry etching. In the first through fifth mask processes described above, the first through fifth photoresist layers P1 to P5 are exposed to light and developed, and the remaining structure is patterned using the developed photoresist layer as a mask. However, in the present embodiment, without using a separate photoresist layer, the third insulating layer 19 formed at least partially of an organic insulating material may be directly dry etched.

[0060] In one embodiment, as shown in FIG. 17, the third insulating layer 19 is dry etched to form a hole H2 through which the pixel electrode 414 is exposed. As a result, a pixel defining layer 419 defining pixels is formed. The pixel defining layer 419 has a predetermined thickness, thereby widening a gap between edges of the pixel electrode 414 and a counter electrode 422 (FIG. 18), thus preventing the occurrence of an electric field concentration phenomenon at the edges of the pixel electrode 414. As a result, the pixel defining layer 419 prevents the pixel electrode 414 and the counter electrode 422 from being short-circuited from each other.

Referring to FIG. 18, an intermediate layer 421 including an organic emissive layer is formed on the exposed portion of the pixel electrode 414 and a portion of the pixel defining layer 419, and the counter electrode 422 is formed on the intermediate layer 421 and the pixel defining layer 419.

[0061] The organic emissive layer of the intermediate layer 421 is electrically driven by the counter electrode 422 to emit light. The organic emissive layer may be formed at least partially of a low molecular or high molecular weight organic compound.

[0062] In one embodiment, when the organic emissive layer is formed of a low molecular weight organic compound, the intermediate layer 421 may include a hole transport layer (HTL) and a hole injection layer (HIL) that are sequentially stacked on the organic emissive layer towards the pixel electrode 414, and an electron transport layer (ETL) and an electron injection layer (EIL) that are sequentially stacked on the organic emissive layer towards the counter electrode 422. Other layers may also be stacked, depending on the embodiment. An organic material used may be copper phthalocyanine (CuPc), N,N-Di(naphthalene-1-yl)-N,N'-diphenylbenzidine (NPB), or tris-8-hydroxyquinoline aluminum (Alq₃).

[0063] In one embodiment, when the organic emissive layer is formed of a high molecular weight organic compound, the intermediate layer 421 may include only the HTL formed on the organic emissive layer towards the pixel electrode 414. The HTL may be formed on the pixel electrode 414 by ink-jet printing or spin coating poly-(2,4)-ethylene-dihydroxy thiophene (PEDOT) or polyaniline (PANI). An organic material used may be a high molecular weight organic compound, such as poly-phenylenevinylene (PPV)-based organic compound or a polyfluorene-based organic compound. Color patterns may be formed using a commonly used method such as by ink-jet printing, spin coating, or heat transfer using a laser.

[0064] The counter electrode 422 is formed on the intermediate layer 421 including the organic emissive layer. In one, the pixel electrode 414 is used as an anode, and the counter electrode 422 is used as a cathode. In another embodiment, the pixel electrode 414 is used as a cathode, and the counter electrode 422 is used as an anode.

[0065] In a top emission type organic light emitting display in which an image is displayed on the opposite side of the substrate 10, the pixel electrode 414 is a reflective electrode, and the counter electrode 422 is a transparent electrode. The reflective electrode may be formed at least partially of a metal with a low work function, such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, LiF/Al, or compounds thereof, in a thin film.

[0066] Although not illustrated in FIG. 18, a sealing element (not shown) and an absorbent element (not shown) may be further formed on the counter electrode 422 to protect the organic emissive layer from external moisture or oxygen.

[0067] According to one embodiment, the organic light emitting display 1 having the above-described structure may be manufactured using a small number of masks, and thus manufacturing costs are reduced. In addition, the manufacturing processes may be simplified, resulting in low manufacturing costs.

[0068] In addition, when a gate insulating layer has a double-layered structure, the roughness of the pixel electrode 414 may be low. For example, in a conventional organic light emitting display (not necessarily prior art), the pixel electrode 414 is disposed below the gate electrode 212 or the source and

drain regions **217a** and **217b**. In such a structure, to expose the pixel electrode **414**, the gate electrode **212** or the source and drain regions **217a** and **217b** need to be etched. In addition, in a doping process of the thin film transistor **2**, the exposed pixel electrode **414** is likely to be doped. These processes increase the surface roughness of the pixel electrode **414**. On the other hand, according to an embodiment, the pixel electrode **414** is disposed between the double-layered gate insulating layer, whereby an increase in the surface roughness of the pixel electrode **414** caused by etching an upper metal electrode may be minimized.

[0069] In addition, when a single gate insulating layer is used, tetraethyl orthosilicate (TEOS) is widely used to form the gate insulating layer. However, when a thickness of a lower metal electrode is large, the step coverage is insufficient by using only TEOS. This is because an increase in the thickness of TEOS to obtain sufficient step coverage causes a change in electrical capacitance. According to at least one embodiment, the gate insulating layer has a double-layered structure, thereby minimizing the change in electrical capacitance. In addition, the step coverage of a lower electrode is enhanced.

[0070] As described above, according to at least one embodiment, the organic light emitting display may be manufactured using a small number of masks, and thus manufacturing costs may be reduced. In addition, the manufacturing processes may be simplified, thereby reducing manufacturing costs.

[0071] While embodiments have been particularly shown and described with reference to the drawings, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

What is claimed is:

1. An organic light emitting display comprising:
 - a gate electrode formed over a substrate;
 - an active layer electrically insulated from the gate electrode;
 - a first gate insulating layer and a second gate insulating layer formed between the gate electrode and active layer so as to electrically insulate the active layer from the gate electrode; and
 - source and drain electrodes each contacting the active layer.
2. The display of claim 1, wherein the active layer is formed at least partially of oxygen and at least one selected from the group consisting of Ga, In, Zn, Hf, and Sn.
3. The display of claim 1, wherein the first gate insulating layer and the second gate insulating layer are formed adjacent to each other.
4. The display of claim 1, wherein the first gate insulating layer covers the gate electrode.
5. The display of claim 1, further comprising:
 - a plurality of pixel electrodes formed on the first gate insulating layer;
 - a plurality of pixel-defining layers formed between the pixel electrodes;
 - a plurality of organic layers formed on the pixel electrodes and the pixel defining layers; and
 - a counter electrode formed on the organic layers.
6. The display of claim 5, wherein the second gate insulating layer contacts i) at least one of the pixel electrodes and ii) at least one of the pixel defining layers.

7. The display of claim 5, wherein at least one of the organic layers contacts the second gate insulating layer.

8. The display of claim 5, wherein the active layer contacts at least one of the pixel-defining layers.

9. The display of claim 1, wherein the source and drain electrodes contact part of the second gate insulating layer.

10. A method of manufacturing an organic light emitting display, the method comprising:

performing a first mask process so as to form a first conductive layer on a substrate and pattern the first conductive layer to form a gate electrode of a thin film transistor;

performing a second mask process so as to form a first insulating layer on the resulting structure obtained according to the first mask process, form a second conductive layer on the first insulating layer, and pattern the second conductive layer to form a pixel electrode;

performing a third mask process so as to form a second insulating layer on the resulting structure obtained according to the second mask process, form a semiconductor layer on the second insulating layer, and pattern the semiconductor layer to form an active layer of the thin film transistor;

performing a fourth mask process so as to remove a portion of the second insulating layer to expose a portion of the pixel electrode;

performing a fifth mask process so as to form a third conductive layer on the resulting structure obtained according to the fourth mask process and pattern the third conductive layer to form source and drain electrodes of the thin film transistor; and

performing a sixth mask process so as to form a third insulating layer on the resulting structure obtained according to the fifth mask process and remove the third insulating layer to expose the pixel electrode.

11. The method of claim 10, wherein the active layer is formed at least partially of oxygen and at least one element selected from the group consisting of Ga, In, Zn, Hf, and Sn.

12. The method of claim 10, wherein the first insulating layer is formed as a first gate insulating layer, wherein the second insulating layer is formed as a second gate insulating layer, and wherein the first gate insulating layer and the second gate insulating layer contact each other.

13. The method of claim 10, further comprising sequentially forming i) an intermediate layer comprising an emissive layer and ii) a counter electrode on the resulting structure obtained according to the sixth mask process.

14. The method of claim 10, further comprising forming a buffer layer between the substrate and the gate electrode, wherein the buffer layer contacts the first gate insulating layer.

15. An organic light emitting display comprising:

- a gate electrode formed over a substrate;
- a first gate insulating layer substantially covering the gate electrode;
- a second gate insulating layer formed on the first gate insulating layer;
- an active layer formed over and contacting the second gate insulating layer; and
- source and drain electrodes formed over and contacting the active layer.

16. The display of claim **15**, further comprising:

a pixel electrode formed on the first gate insulating layer, wherein at least part of the pixel electrode is interposed between the first and second gate insulating layers;

an organic light emission layer formed on the pixel electrode; and

a counter electrode formed on the organic light emission layer.

17. The display of claim **16**, further comprising a pixel-defining layer formed between the second gate insulating layer and organic light emission layer, wherein the pixel-

defining layer covers i) the source and drain electrodes, ii) part of the active layer and iii) part of the second gate insulating layer.

18. The display of claim **15**, wherein the first and second gate insulating layers have substantially the same thickness.

19. The display of claim **15**, wherein the active layer covers at least part of the second gate insulating layer, and wherein the active layer is farther from the substrate than the first and second gate insulating layers.

20. The display of claim **15**, wherein the first gate insulating layer does not contact the pixel-defining layer.

* * * * *

专利名称(译)	有机发光显示器及其制造方法		
公开(公告)号	US20110140112A1	公开(公告)日	2011-06-16
申请号	US12/881686	申请日	2010-09-14
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	KIM MIN KYU KANG JAE WOOK		
发明人	KIM, MIN-KYU KANG, JAE-WOOK		
IPC分类号	H01L51/52 H01L51/56		
CPC分类号	H01L27/3248		
优先权	1020090125685 2009-12-16 KR		
其他公开文献	US8890148		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种有机发光显示器及其制造方法。在一个实施例中，显示器包括形成在衬底上的栅电极和与栅电极电绝缘的有源层，其中栅电极比有源层更靠近衬底。显示器还包括：i) 第一栅极绝缘层和形成在栅电极和有源层之间的第二栅极绝缘层，以使有源层与栅电极电绝缘；和ii) 每个与有源层接触的源电极和漏电极。

